METHOD AND TESTING CIRCUIT FOR TRACKING TRANSISTOR STRESS DEGRADATION

Abstract of the Disclosure

A method and testing circuit are provided for tracking transistor stress degradation. A first array of P-channel field effect transistors (PFETs) is connected in parallel. The first array of PFETs is stressed by applying a low gate input and a high source and a high drain to the PFETs during a stress period. The first array of PFETs is tested by operating the PFETs in a saturated region during a test period. A reference array of PFETs is not stressed during the stress period. The reference array of PFETs is activated for testing to compare a saturated drain current performance with the first array of PFETs during the test period.